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-- This application is a divisional of U.S. patent application Serial No. 09/059,590, now U.S. Patent No. 6,288,423.--

Please amend pages 6-9 of the specification as shown on the attached sheets.

IN THE CLAIMS

Kindly cancel claim 37, without prejudice or disclaimer, and amend claims 28, 32, 33, 36, 38, and 42 to read as follows:

28. (Amended) A method of fabricating a semiconductor device, comprising:

the first step of defining an element active region by forming an element isolation structure on a semiconductor substrate;

the second step of forming an insulating film on said semiconductor substrate in said element active region;

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the third step of forming a first conductive film on an entire surface of said semiconductor substrate including said insulating film and said element isolation structure;

the fourth step of forming a mask pattern having first and second openings on said first conductive film;

the fifth step of etching said first conductive film until said element isolation structure is exposed in said first opening by using said mask pattern as a mask, thereby dividing said first conductive film, and simultaneously forming a recess in said second opening where said first conductive film forms a bottom of said recess;

the sixth step of forming a dielectric film so as to cover a surface of said first conductive film; and

the seventh step of forming a second conductive film on said dielectric film opposing said first conductive film through said dielectric film.

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32. (Amended) A method of fabricating a semiconductor device, comprising:

the first step of defining an element active region by forming an element isolation structure on a semiconductor substrate;

the second step of forming a gate insulating film and a gate electrode in said element active region;

the third step of doping an impurity into said active region of said substrate to form a pair of impurity diffusion layers in surface regions of said semiconductor substrate on two sides of said gate electrode;

the fourth step of forming a first conductive film electrically connected to one of said impurity diffusion layers;

the fifth step of forming a mask pattern having at least first and second openings on said first conductive film;

the sixth step of etching said first conductive film by using said mask pattern as a mask until said first opening extends to said element isolation structure, thereby dividing said first conductive film in said first opening, and simultaneously forming a recess in said second opening having said first conductive film forming a bottom of said recess;

the seventh step of forming a dielectric film so as to cover a surface of said first conductive film; and

the eighth step of forming a second conductive film on said dielectric film opposing said first conductive film through said dielectric film.

33. (Amended) A method according to claim 32, further comprising, between the third and fourth steps,

the ninth step of forming an insulating interlayer on an entire surface of said semiconductor substrate, and

the tenth step of forming a hole in said insulating interlayer in which one of said impurity diffusion layers is exposed, and

B3 Cont'd wherein in the fourth step, a first conductive film is formed on said insulating interlayer and said hole is filled with said first conductive film.

sub E2 36. (Amended) A method of fabricating a semiconductor device, comprising:

the first step of forming a first conductive film in an insulating film region on a semiconductor substrate;

the second step of forming a mask pattern having two openings of different dimensions on said first conductive film;

the third step of etching said first conductive film by using said mask pattern as a mask, thereby dividing said first conductive film conforming to a shape of one of said openings so as to reach said insulating film region, thereby forming a hole in which a surface of said insulating film region is exposed, and simultaneously forming at least one recess in a surface of said divided first conductive film conforming to a shape of the other opening;

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the fourth step of forming an insulating film so as to cover a surface of said first conductive film; and

the fifth step of forming a second conductive film so as to cover a surface of said insulating film opposing said first conductive film through said insulating film.

sub E3 38. (Amended) A method of fabricating a semiconductor device, comprising:

the first step of defining an element active region by forming an element isolation structure on a semiconductor substrate;

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the second step of forming an insulating film on said semiconductor substrate in said element active region;

the third step of forming a first conductive film on an entire surface including said insulating film and said element isolation structure;

the fourth step of forming a mask pattern having at least first and second openings on said first conductive film;

the fifth step of etching said first conductive film until said element isolation structure is exposed in said first and second openings by using said mask pattern as a mask, thereby dividing said first conductive film below said first opening, and simultaneously forming a hole extending through said first conductive film below said second opening;

the sixth step of forming a dielectric film so as to cover said first conductive film; and

the seventh step of forming a second conductive film on said dielectric film and opposing said first conductive film through said dielectric film.

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42. (Amended) A method of fabricating a semiconductor substrate, comprising:

the first step of defining an element active region by forming an element isolation structure on a semiconductor substrate;

the second step of forming a gate oxide film and a gate electrode on said semiconductor substrate in said element active region;

the third step of doping an impurity into said semiconductor substrate in said element active region to form a pair of impurity diffusion layers in surface regions of said semiconductor substrate on two sides of said gate electrode;

the fourth step of forming a first conductive film electrically connected to one of said impurity diffusion layers;

the fifth step of forming a mask pattern having at least first and second openings on said first conductive film;

the sixth step of etching said first conductive film by using said mask pattern as a mask, thereby dividing said first conductive film below said first opening, and simultaneously forming a hole extending through said first conductive film below said second opening, said first conductive film is etched until said insulating interlayer is exposed in said first opening;